

CANopen powers subway auxiliary inverters

Leroy introduces how to implement some key features of auxiliary inverters' management onto commercial-off-the-shelf (COTS) technologies: the Brio hardware platform. In the context of the New York City Transit – R211 subway project, the platform acts as a remote input/output module based on CANopen.

Leroy Automation is manufacturer of automation systems for on-board train and rail signaling control-command systems. For several decades, they have been accompanying major rolling stock manufacturers, locomotive subsystem integrators, and original equipment suppliers for rolling stock vehicles as well as for many train fleet overhaul projects.

As part of on-board train architectures, energy management is an important topic where efficient power converters are key subsystems. Thanks to the auxiliary power converters or inverters, the current-voltage characteristics



Figure 1: The Brio R107 CANopen-based PLC (Source: Leroy)

can be adjusted to match the requirements of subsystems installed into subway cars and railway vehicles. They also fulfil a significant role in safety by protecting the entire system, as they are resistant to over-voltages and short-circuits. The intelligence of the auxiliary inverters is implemented onto powerful embedded controllers, where high-speed digital signal processing tasks are common.

The hardware platform

Brio is an Ethernet-based decentralized-remote input/output module, designed to be embedded on-board in rolling stock vehicles. It is available as a product range offering different digital and analog inputs/outputs configurations, and several communication interfaces such as CAN, Ethernet, EIA-485, MVB, etc. In general, Brio finds its use cases in embedded railway systems like a programmable logic controller (PLC) or a remote input/output module (RIOM); where digital and analog I/Os are managed from one or several communication ports. Nevertheless, its internal hardware architecture is based on a powerful STM32 micro-controller and an FPGA device, which makes it suitable for various applications.

In the context of the New York City Transit – R211 subway project, the platform acts as a remote input/output module based on CANopen. Fully compliant with the EN 50155 railway standard, it counts not less than 55 I/O signals on a thin size-6U board footprint. It is the ideal COTS solution to be integrated in train propulsion systems. In parallel, the

company has been asked to think about an innovative solution for the Brio to be able to detect in real-time a ripple voltage on a high-voltage DC line around 900 V_{DC}. The technical specification was restrictive: the AC ripple signal can range from 0,35 V_{rms} to 70 V_{rms}, and can be on any two frequencies between 0 kHz and 1 kHz. In addition, the system had to be fully configurable and monitored from the CANopen interface (ripple frequencies to be detected, detection temporal window, V_{rms} threshold to declare the ripple present or not, measured energy for both frequencies), and had to activate specific digital outputs on frequency detection.

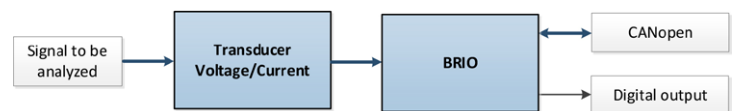


Figure 2: The final system solution could be presented as the following system-level block diagram (Source: Leroy)

In digital signaling processing (DSP), the DFT (discrete fourier transform) is a tool to find a specific frequency in a signal. Simulations have shown that a DFT linked to Hann windows, gave good results with an acceptable accuracy on signals recorded on train. The DFT equation by itself is not so complex:

$$X(k) = \sum_{t=0}^{N-1} x(t) e^{-i \frac{2\pi k}{N} t}$$

It just says that “X(k)” is the level of the frequency “k” in the complete signal represented by a set of “N” samples “x(t)” of the analyzed signal.

The Hann window consists in deforming the analyze signal before applying the DFT algorithm. Indeed, the DFT implies a temporal windowing of the signal over N samples, which affects the signal spectrum. Applying a pre-deformation such as Hann windows prior to the DFT improve the frequency response of the DFT.

The Hann window is also not very complex in terms of digital signal processing function. For a set of N samples, it gives a coefficient to apply on the sample “t” by the following formula:

$$w(t) = 0.5 \times \left[1 - \cos \left(\frac{2\pi t}{N} \right) \right]$$

In order to illustrate the efficiency of the Hann window, let's take a pure sinus signal. ▶

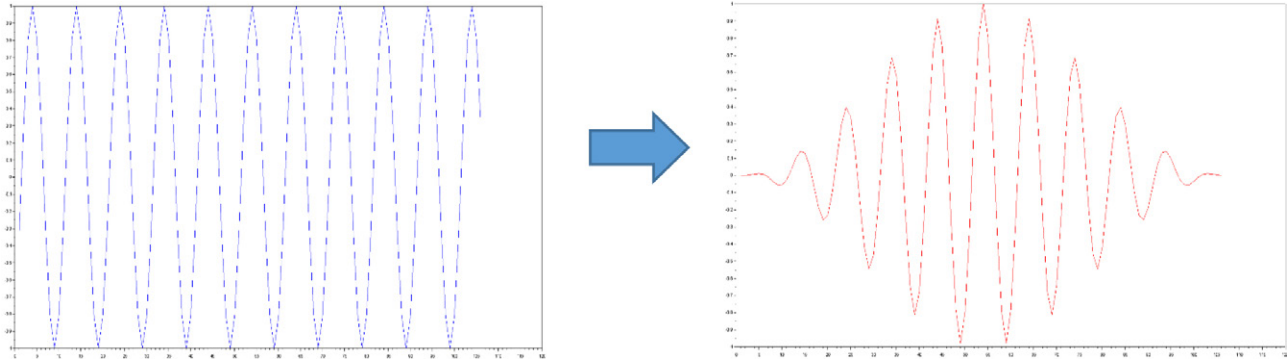


Figure 3: Representation of Hann function in time domain (Source: Leroy)

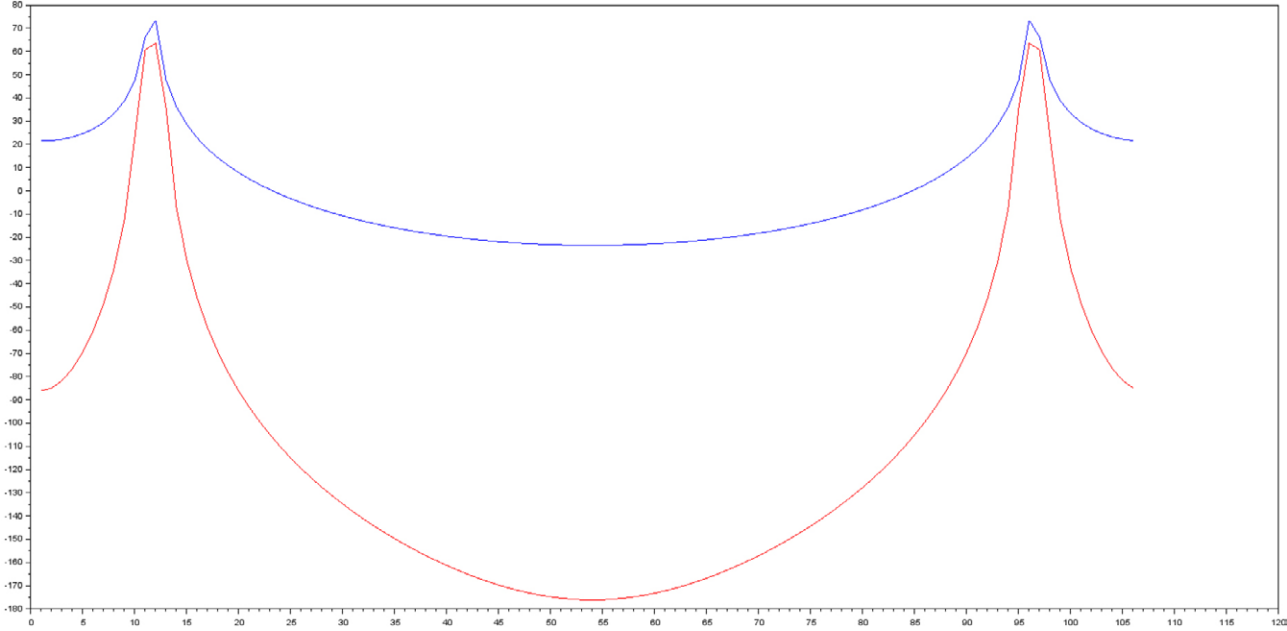


Figure 4: Representation of Hann function in frequency domain (Source: Leroy)

We can see that in frequency domain, the spectrum representation gives much better results with Hann window than without. Indeed, the energy peaks that characterize the harmonics of the original signal are much clearer in red, which allows a frequency detection with a better accuracy. Thus, in order to detect two specific frequencies “K1” and “K2” in the analyzed signal, the algorithm to implement can be seen in Figure 5.

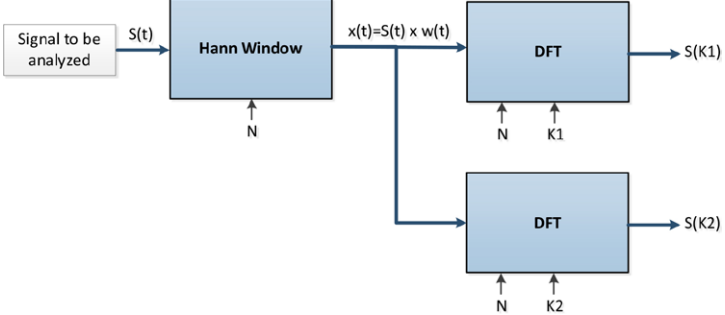
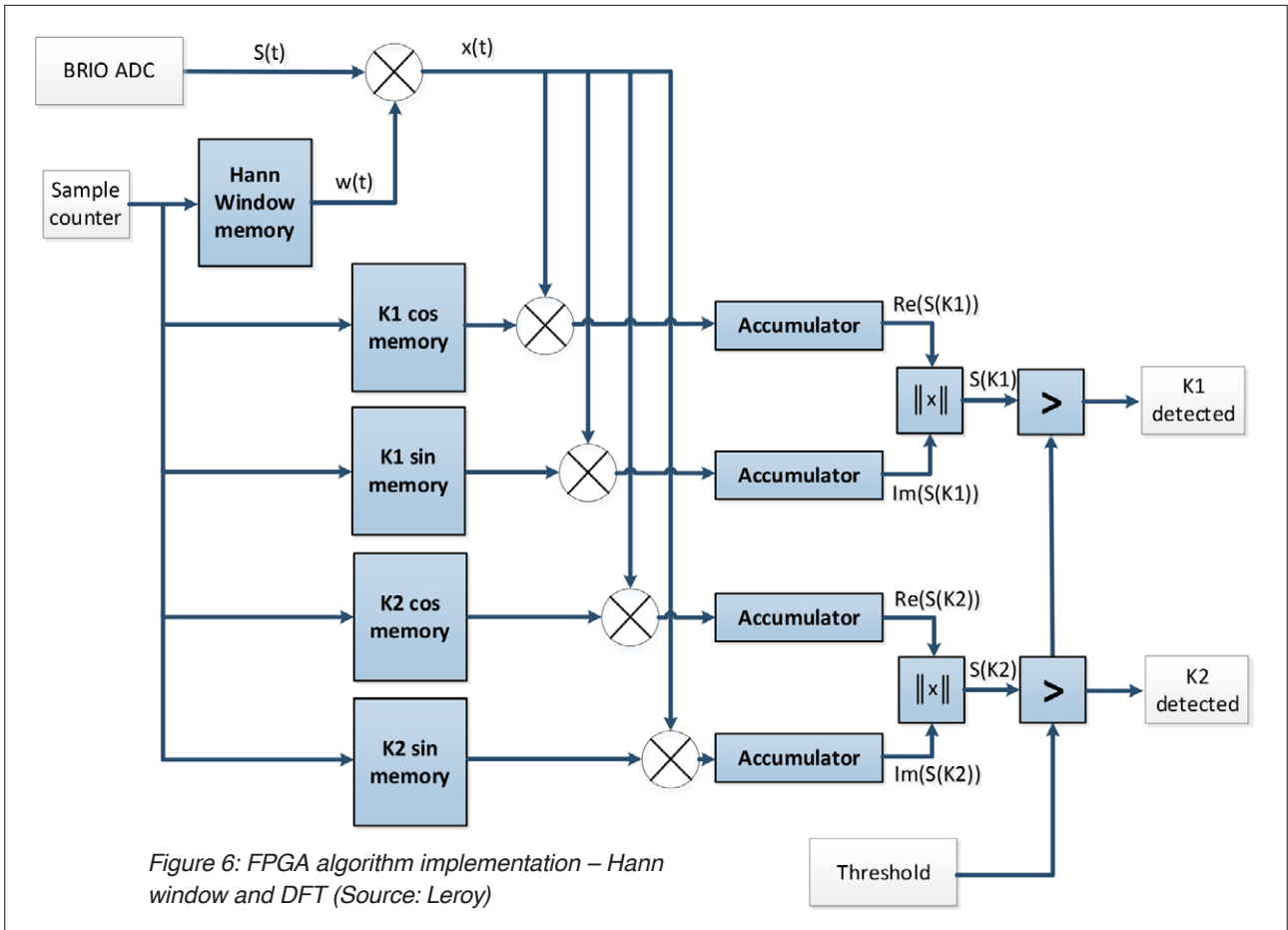


Figure 5: Digital signal processing – Hann window and discrete fourier transforms (DFT) (Source: Leroy)

It is one thing to make an offline simulation on a Windows-based PC, with mathematical tools. But it is another challenge to make the same in real-time, in an on-board PLC, with the very same accuracy.

As mentioned earlier, the Brio is based on a STM32 micro-controller and an FPGA device. It could have been easy to implement the algorithm in the micro-controller. A few ANSI-C programming lines would have been enough. Nevertheless, the micro-controller was already busy to manage the other functionalities of the Brio itself, including CANopen messages, and the real-time criteria would have been difficult to meet. It was then decided to implement the algorithm in the FPGA device. At this point, the difficulty remains in implementing calculus in the hardware chip. Indeed FPGAs, and specifically small matrices, are not adapted well for floating-point computing with cosine and sine functions. The idea was to take benefit of each device strength with a modular design approach: micro-controller for complex floating-point and cosine/sine off-line calculus, FPGA for real-time fixed-point computing. The real-time part of the algorithm implemented in the FPGA can be represented as shown in Figure 6.

Each time a parameter is modified (window size, K1, K2, sampling frequency), the micro-controller computes only once the five tables that contain cosine and sine coefficients needed by the Hann window and the DFT. Furthermore, the FPGA only needs to perform simple operations such as multiplications and additions, for which it is very well suited. The digital part of the algorithm worked fine but a challenge remains. The signal to analyze is composed of a DC part that can be up to 1000 V_{DC}. On the other hand, the ripple ▶



can be as low as $0,5 V_{AC}$. It was necessary to remove the DC part of the signal in order to keep most of the ADC (analog digital converter) resolution for the AC part. It was also necessary to keep the low-pass filter required before any analog-to-digital conversion. The resulting band-pass filter has then required a lot of calculus and simulations to be flat enough over the required frequency range, and for the whole temperature range (from $-40\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$). It had also to fit the small footprint available on the Brio printed-circuit board (PCB). At the end, we were able to modify one analog input of the Brio to implement the band-pass filter shown in Figure 7.

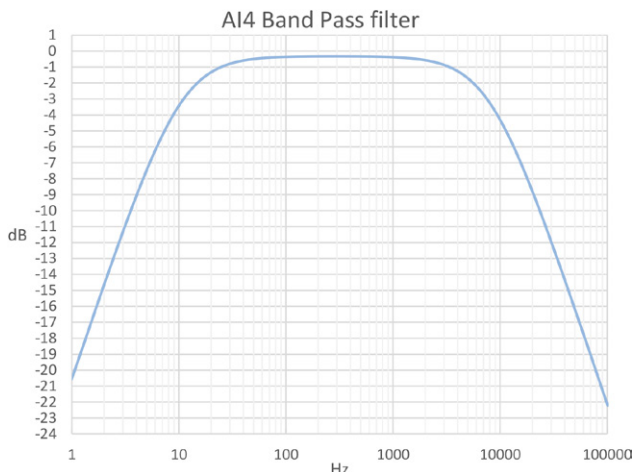


Figure 7: Implementation of band-pass filter in FPGA device (Source: Leroy)

At this time, interfacing the frequency detection system with the CANopen stack was the easiest part of the project. Some specific PDO messages have been implemented to configure dynamically the detection parameters and to report the detection results in a very efficient way.

As a conclusion, this project has been a great engineering success. Operational tests on-board subway cars gave excellent results, totally in line with theory and simulations. Brio was already known as a highly available and reliable I/O module with PLC-programming capabilities. But this particular auxiliary inverter application has revealed all the potential and benefits of the Brio hardware with the partitioning of digital signaling processing algorithms and techniques onto a mixed FPGA and micro-controller platform.

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